

ABSTRACT

New compositions and methods for electrolytic deposition of metal layers, including metal traces, (e.g. circuit patterns) that are electrically segregated from adjacent traces in an electronic device, such as a semiconductor wafer or a printed circuit board. The invention includes providing the segregated traces by compositionally modulated plating methods, i.e. for example where a single plating bath (electrolyte) is employed to deposit two different metals at differing current densities or reduction potentials.

BOS2_180987.1

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100